WHAT IS CLAIMED IS:

1. A method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a substrate;

forming an insulating film such that the conductive film is covered with the insulating film;

forming, in the insulating film, a hole having a bottom portion not reaching the conductive film by using a mask having a first opening pattern; and

forming, in the insulating film, an opening for exposing the conductive film by using a mask having a second opening pattern having an opening diameter larger than an opening diameter of the first opening pattern,

an obtuse angle being formed between a wall surface of the opening and a bottom surface of the opening.

2. The method of claim 1, further comprising the step of:

forming, at least in the opening, a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode.

3. The method of claim 2, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

4. The method of claim 3, wherein each of the lower electrode and the upper electrode contains a platinum group element as a main component.

5. The method of claim 3, wherein the capacitor insulating film is composed of a

ferroelectric film or a high dielectric film.

6. The method of claim 3, wherein the capacitor insulating film is composed of $SrBi_2(Ta_xNb_{1-x})_2O_9$, $Pb(Zr_xTi_{1-x})O_3$, $(Ba_xSr_{1-x})TiO_3$, $(Bi_xLa_{1-x})_4Ti_3O_{12}$ (where X satisfies a relationship represented by $0 \leq x \leq 1$), or Ta_2O_5.

7. The method of claim 3, wherein the conductive film is composed of iridium, platinum, gold, ruthenium, rhodium, palladium, or a metal oxide thereof or alternatively composed of titanium, titanium-aluminum, tantalum, tantalum-aluminum, a nitride thereof, or a multilayer film composed thereof.

8. The method of claim 3, wherein the conductive film contains an oxygen barrier film.

9. The method of claim 3, wherein the insulating film is an oxide film containing silicon.

10. The method of claim 3, wherein the insulating film has a planarized principal surface.

11. The method of claim 3, wherein the mask is a photoresist.

12. A method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a specified region of a substrate;

forming an insulating film on the substrate such that the conductive film is covered with the insulating film;

forming, on the insulating film, a mask having a first opening pattern above the conductive film;

performing first etching with respect to the insulating film by using the mask having the first opening pattern to form, in the insulating film, a depressed portion having a bottom portion not reaching the conductive film;

forming a mask having a second opening pattern having an opening diameter larger than an opening diameter of the first opening pattern by enlarging the opening diameter of the first opening pattern; and

performing second etching with respect to the insulating film by using the mask having the second opening pattern to form, in the insulating film, an opening for exposing the conductive film such that the opening has a diameter larger than a diameter of the depressed portion and a wall surface having a tapered configuration.

13. The method of claim 12, further comprising the step of:

forming, at least in the opening, a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode.

14. The method of claim 13, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

15. The method of claim 12, further comprising, between the step of forming the mask having the first opening pattern and the step of forming the depressed portion in the insulating film, the step of:

forming a wall surface of the first opening pattern into a tapered configuration.

16. The method of claim 12, further comprising, after the step of forming the opening in the insulating film, the step of:

after removing the mask, performing third etching with respect to an entire surface of the insulating film to smooth the tapered configuration of the wall surface of the opening.

17. The method of claim 12, further comprising, after the step of forming the opening in the insulating film, the steps of:

forming a mask having a third opening pattern having an opening diameter larger than the opening diameter of the second opening pattern by enlarging the opening diameter of the second opening pattern; and

performing third etching with respect to the insulating film by using the mask having the third opening pattern to smooth the tapered configuration of the wall surface of the opening.

18. The method of claim 16 or 17, further comprising, after the step of smoothing the tapered configuration of the wall surface of the opening, the step of:

forming, at least in the opening, a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode.

19. The method of claim 18, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

20. A method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a specified region of a substrate;

forming an etching stopper film on the conductive film;

forming an insulating film on the substrate such that the etching stopper film is covered with the insulating film;

forming, on the insulating film, a mask having a first opening pattern above the

conductive film;

performing first etching with respect to the insulating film by using the mask having the first opening pattern to form, in the insulating film, a depressed portion having a bottom portion not reaching the etching stopper film;

forming a mask having a second opening pattern having an opening diameter larger than an opening diameter of the first opening pattern by enlarging the opening diameter of the first opening pattern;

performing second etching with respect to the insulating film by using the mask having the second opening pattern to form, in the insulating film, an opening for exposing the etching stopper film such that the opening has a diameter larger than a diameter of the depressed portion and a wall surface having a tapered configuration; and

performing third etching with respect to the etching stopper film to transfer the opening of the insulating film to the etching stopper film and thereby form, in the etching stopper film, an opening for exposing the conductive film, while smoothing the tapered configuration of the wall surface of the opening of the insulating film.

21. The method of claim 20, further comprising the step of:

forming a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode at least in the opening of the insulating film and in the opening of the etching stopper film.

22. The method of claim 21, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

23. The method of claim 20, wherein the third etching is performed after removing the mask.

24. The method of claim 20, wherein the third etching is performed by using a mask having a third opening pattern formed by enlarging the opening diameter of the second opening pattern.

25. The method of claim 20, further comprising, between the step of forming the mask having the first opening pattern and the step of forming the depressed portion in the insulating film, the step of:

forming a wall surface of the first opening pattern into a tapered configuration.

26. The method of claim 20, wherein the etching stopper film is composed of a metal oxide containing titanium or aluminum.

27. A method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a specified region of a substrate;

forming an insulating film on the substrate such that the conductive film is covered with the insulating film;

forming, on the insulating film, a mask having a first opening pattern above the conductive film;

performing first etching with respect to the insulating film by using the mask having the first opening pattern to form, in the insulating film, a depressed portion having a bottom portion not reaching the conductive film; and,

after removing the mask, performing second etching with respect to an entire surface of the insulating film to form, in the insulating film, an opening for exposing the conductive film such that the opening has a diameter larger than a diameter of the depressed portion and a wall surface having a tapered configuration.

28. The method of claim 27, further comprising the step of:

forming, at least in the opening of the insulating film, a capacitor element composed of a lower electrode, a capacitor insulating film, and an upper electrode.

29. The method of claim 28, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode;

forming the capacitor insulating film on the lower electrode; and

forming the upper electrode on the capacitor insulating film.

30. The method of claim 27, further comprising, between the step of forming the mask having the first opening pattern and the step of forming the depressed portion in the insulating film, the step of:

forming a wall surface of the first opening pattern into a tapered configuration.